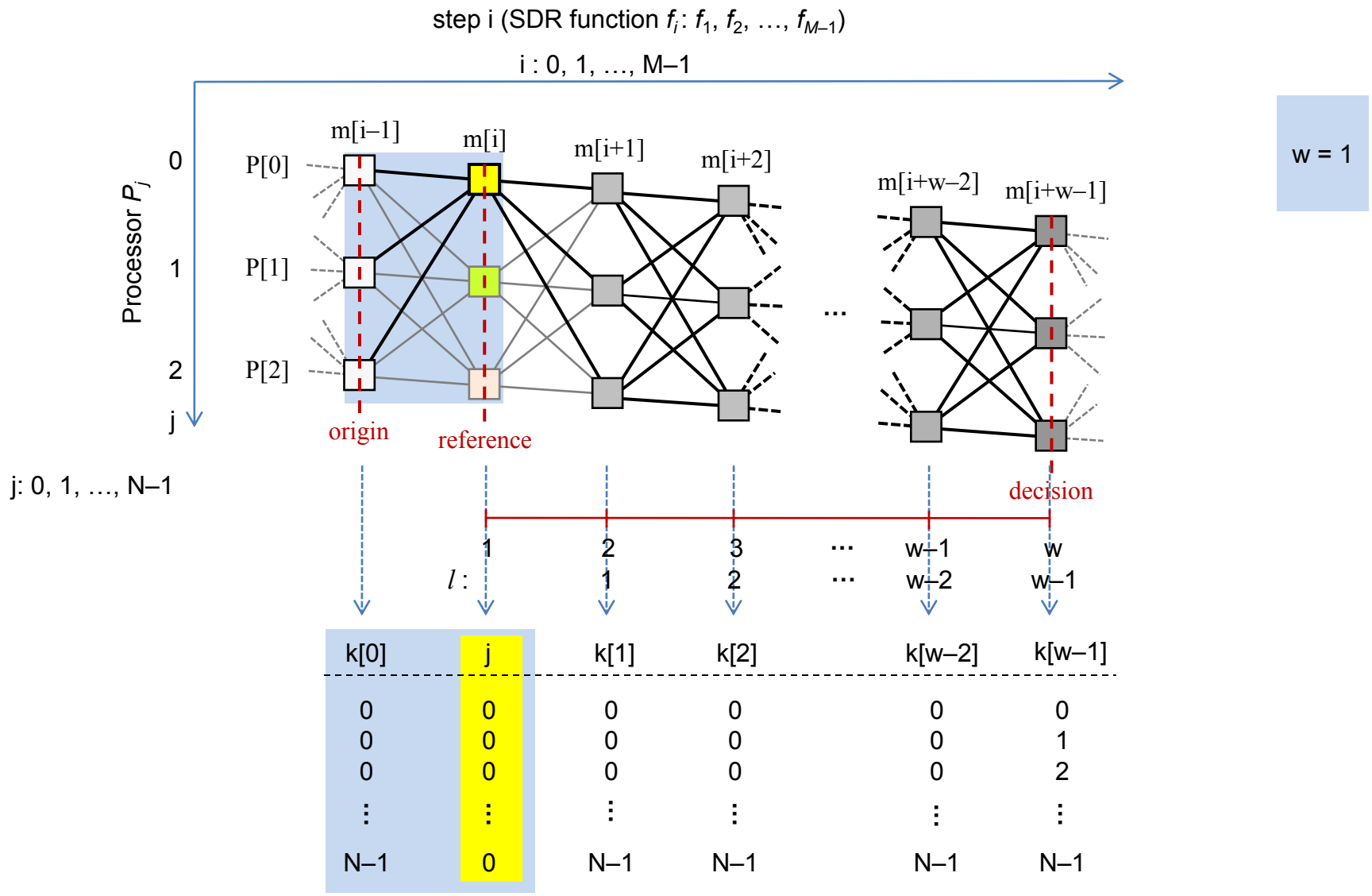
Implementation Details

The following slides explain the concepts and indices of the *tw_mapping.c* and *gw_mapping.c* files, implementing the t_w-mapping and g_w-mapping algorithms.

t_w-mapping

m[i] : processing requirement of SDR function f_i
P[j] : processing powers of processor P_j



t_w-mapping

w-paths	[P[k[0]]	P[j]	P[k[1]]	P[k[2]]	⋯	P[k[w–1]]]
	0	0	0	0	⋯	0
	0	0	0	0	⋯	1
	0	0	0	0	⋯	2
t-node $\{P[j] = 0, f_i\}$			⋮			
	0	0	0	0	⋯	N–1
			⋮			
	N–1	0	N–1	N–1	⋯	N–1

w-paths	[P[k[0]]	P[j]	P[k[1]]	P[k[2]]	⋯	P[k[w–1]]]
	0	1	0	0	⋯	0
	0	1	0	0	⋯	1
	0	1	0	0	⋯	2
t-node $\{P[j] = 1, f_i\}$			⋮			
	0	1	0	0	⋯	N–1
			⋮			
	N–1	1	N–1	N–1	⋯	N–1

⋮

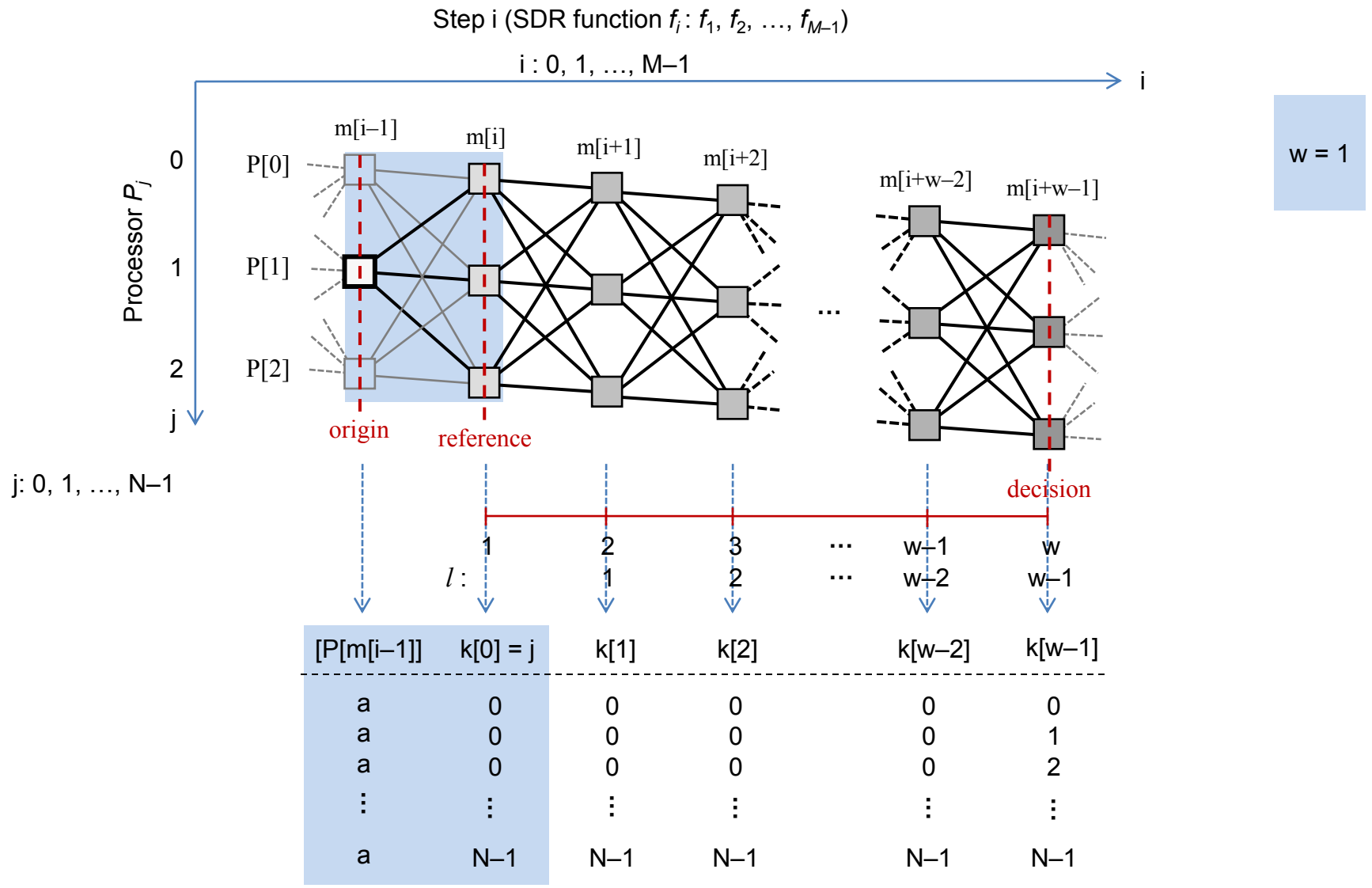
Example: w = 3, N = 3

w-paths	[P[k[0]]	P[j]	P[k[1]]	P[k[2]]]
	0	0	0	0
	0	0	0	1
	0	0	0	2
	0	0	1	0
	0	0	1	1
	0	0	1	2
	0	0	2	0
	0	0	2	1
	0	0	2	2
	1	0	0	0
	1	0	0	1
	1	0	0	2
	1	0	1	0
	1	0	1	1
	1	0	1	2
	1	0	2	0
	1	0	2	1
	1	0	2	2
	2	0	0	0
	2	0	0	1
	2	0	0	2
	2	0	1	0
	2	0	1	1
	2	0	1	2
	2	0	2	0
	2	0	2	1
	2	0	2	2

$N^w = 3^3 = 27$ w-paths for each t-node at step i

g_w-mapping

m[i] : processing requirement of SDR function f_i
P[j] : processing powers of processor P_j



a represents the active processor at step i–1. There is a single active *t*-node {P[m[m[i–1], m[i–1]} = {a, m[i–1]}

g_w-mapping

w-paths	[P[m[i-1]]	P[k[0]]	P[k[1]]	P[k[2]]	⋯	P[k[w–1]]]
	a	0	0	0	⋯	0
	a	0	0	0	⋯	1
	a	0	0	0	⋯	2
			⋮			
	a	0	0	0	⋯	N–1
			⋮			
	a	0	N–1	N–1	⋯	N–1

a: active processor at step *i*–1

Example: w = 3, N = 3

w-paths	[P[m[i-1]]	P[j]	P[k[1]]	P[k[2]]]
	a	0	0	0
	a	0	0	1
	a	0	0	2
	a	0	1	0
	a	0	1	1
	a	0	1	2
	a	0	2	0
	a	0	2	1
	a	0	2	2
	a	1	0	0
	a	1	0	1
	a	1	0	2
	a	1	1	0
	a	1	1	1
	a	1	1	2
	a	1	2	0
	a	1	2	1
	a	1	2	2
	a	2	0	0
	a	2	0	1
	a	2	0	2
	a	2	1	0
	a	2	1	1
	a	2	1	2
	a	2	2	0
	a	2	2	1
	a	2	2	2

$N^w = 3^3 = 27$ *w*-paths between the active *t*-node at step i–1 and the *t*-nodes at step *i*+*w*–1